

EXPRESS MAIL NO. EV343427593US

DATE MAILED: JULY 2, 2003

PATENT

INVENTORS: Adalberto MARIANI and Giulio CORVA

5

**FREQUENCY/SIGNAL CONVERTER AND
SWITCHING REGULATOR HAVING SUCH A CONVERTER**

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is based upon and claims priority from European Patent
10 Application No. 02425435.1, filed July 2, 2002, the entire disclosure of which is
herein incorporated by reference.

BACKGROUND OF THE INVENTION

1. Field of the Invention

15 The present invention relates to electronic circuits, and more specifically to a
frequency/signal converter and a switching regulator having such a frequency/signal
converter.

2. Description of Related Art

20 In the electronics field, circuits adapted to generate signals that are
proportional to the clock frequency of electronic devices are often employed.
Typically circuits employing conventional phase-locked loops (PLL) are used. A
conventional PLL includes a phase detector of an input signal, a filter, an amplifier,
and a voltage controlled oscillator (VCO). When the lock occurs, the VCO control
25 voltage is made proportional to the frequency of the input signal.

Frequency/signal converters can be utilized in other applications such as in
switching regulators. These regulators provide a substantially constant output voltage
to a load from a fluctuating input voltage, and include a switch, for example a
transistor, coupled in series or in parallel with the load and a filter, usually an LC
30 filter. Generally these transistors are driven by circuitry that controls the turning off

EXPRESS MAIL NO. EV343427593US

and the turning on of the transistor through the definition of a duty-cycle (that is, the rate between the time that the switch is on and the total switching time). Such circuitry usually includes an input clock signal derived from an oscillator that fixes the switching time. A control circuit placed in feedback between the output and the input
5 of the regulator makes the output voltage stable against load variances and input voltage fluctuations.

In the case of current mode switching regulators (that is, regulators controlled by a current signal), the control circuitry takes the current flowing through an inductance and compares it with a current derived from a transconductance amplifier
10 that receives the output voltage of the regulator and a voltage reference. The control circuitry acts on the turning on and off circuitry of the transistor. When the duty-cycle exceeds 50%, current mode switching regulators become unstable. For this reason, a slope compensation signal is injected into the current control signal.

One current mode switching regulator is described in U.S. Patent No.
15 5,929,620. This switching regulator is synchronized by an external clock signal and includes a PLL circuit that synchronizes the oscillator of its VCO with the external clock signal. The phase locked loop synchronizes the oscillator of the VCO without interfering with a slope compensation signal produced by the same VCO and which is added to the current control signal. However, the PLL circuit is not stable and it is
20 necessary to make it stable by adding a compensation network.

SUMMARY OF THE INVENTION

In view of these drawbacks, it is an object of the present invention to overcome the above-mentioned drawbacks and to provide a frequency/signal
25 converter that is simpler than conventional converters.

One embodiment of the present invention provides a frequency/signal converter that receives an input clock signal and generates an output signal. The converter includes a first circuit, a loop circuit, and an integrator device. The first circuit receives the input clock signal and generates first and second logic signals that
30 are complementary with one another. The loop circuit includes a first circuit line and

EXPRESS MAIL NO. EV343427593US

a second circuit line that are each coupled between a first supply voltage and a second supply voltage. A current proportional to the output signal of the converter flows in the loop circuit. The first circuit line includes a first capacitive element, and a first switch for interrupting current flow into the first capacitive element. The second
5 circuit line includes a second capacitive element, and a second switch for interrupting current flow into the second capacitive element. The first switch is controlled by the first logic signal, and the second switch is controlled by the second logic signal. The first and second circuit lines are alternatively coupled to an input terminal of the integrator device in order to obtain a substantially constant voltage signal at the input
10 terminal of the integrator device, and the integrator device provides the output signal of the converter.

Another embodiment of the present invention provides a switching regulator for providing a regulated voltage to a load. The regulator includes a first transistor, at least one inductance, first and second circuits, a control circuit, and a device. The first
15 transistor has a first terminal coupled to an input terminal and a second terminal coupled to the output terminal of the regulator, and the inductance is coupled between the second terminal of the transistor and the output terminal of the regulator. The first circuit is coupled to the output terminal and provides a feedback signal that is representative of the regulated voltage. The second circuit is coupled to the
20 inductance and provides a second signal that is representative of the current flowing through the inductance. The control circuit receives an input clock signal and drives the first transistor so as to interrupt a current flow from the input terminal to the output terminal according to a predetermined duty-cycle. The device receives the input clock signal and generates a slope compensation signal that is proportional to
25 the frequency of the input clock signal when the duty-cycle exceeds a predetermined value. The slope compensation signal is coupled to the control circuit. In one preferred embodiment, the regulator also includes a comparator for comparing a sum of the feedback signal and the slope compensation signal with the second signal.

The present invention makes it possible to form a frequency/signal converter that is stable without a compensation network. The converter can be used to generate a slope compensation signal in a switching regulator.

Other objects, features and advantages of the present invention will become
5 apparent from the following detailed description. It should be understood, however,
that the detailed description and specific examples, while indicating preferred
embodiments of the present invention, are given by way of illustration only and
various modifications may naturally be performed without deviating from the present
invention.

10

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a circuit diagram of a frequency/signal converter according to a preferred embodiment of the present invention;

Figure 2 shows timing diagrams of signals in the converter of Figure 1;

15 Figure 3 shows timing waveforms of the output voltage signal and signals at
some nodes of the converter circuit of Figure 1;

Figure 4 is a circuit diagram of an exemplary current mode buck converter that includes the converter circuit of Figure 1;

Figure 5 shows a comparison between signals in two successive time periods;
20 and

Figure 6 shows timing diagrams of signals that were derived from simulations.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Preferred embodiments of the present invention will be described in detail
25 hereinbelow with reference to the attached drawings.

Figure 1 shows a frequency/signal converter according to one embodiment of the present invention. The converter circuit includes a flip-flop 1 of the toggle type which generates, from a synchronization signal or clock signal Clk (that is, a square wave signal having a period T which is preferably derived from an oscillator), two
30 logic signals PH1 and PH2 which are complementary with each other in a time period

2T, and two pulse signals RESET1 and RESET2 which are sensitive to the respective rising edges of the logic signals PH1 and PH2. These signals are shown in Figure 2.

The converter circuit also includes two lines A and B which have respective switch couples 2 and 3 and 4 and 5. The lines A and B are in parallel to each other and are arranged in a supply path between a supply voltage VDD and ground. The line intermediate nodes C and H are connected with the terminals of two switches 6 and 7, which have their other terminals in common at a node G. Node G is connected with the inverting input of a transconductance error operational amplifier 8 that has a transconductance gain g_m , and the non-inverting input is connected with a reference voltage V_{ref} . The output current from the amplifier 8 is integrated by a capacitor C_{int} , which is connected between the output terminal of the amplifier 8 and ground, in order to produce a voltage V_{cur} . This voltage V_{cur} is input to a transconductor circuit I_K that is adapted to generate a current I , which flows in the lines A and B and which is obtained by $I = K_c * V_{cur}$. The nodes C and H are connected with two capacitor C_{r1} and C_{r2} which have the same value C_r and have their other terminals connected to ground.

The logic signals PH1 and PH2 drive the switches 2 and 7 and 4 and 6, respectively. The pulse signals RESET1 and RESET2 drive the switches 3 and 5, respectively. When the logic signal PH1 is at logic level 1, after the pulse signal RESET1 has discharged to ground the capacitor C_{r1} by closing switch 3, the same capacitor is charged by closing switch 2 for a time period T . The voltage at node C is $V_C = I * T / C_r$. When the logic signal PH2 is at level logic 1, the voltage V_C is applied at the inverting input of the amplifier 8 and after the pulse signal RESET2 has discharged to ground the capacitor C_{r2} by closing switch 5, the same capacitor is charged by closing switch 3 for a time period T . The voltage at node H is always $V_H = I * T / C_r$.

Therefore at the inverting input terminal of the amplifier 8, there is always a voltage $V_G = I * T / C_r$. The difference between the voltages V_G and V_{ref} is integrated in the capacitor C_{int} to obtain a voltage V_{cur} . Since a certain transitory it is obtained

EXPRESS MAIL NO. EV343427593US

that, at the stationary state, $V_g = V_{ref}$ and from this $I = C_r * V_{ref} * f$. Therefore it is evident that the current I is proportional to the frequency $f = 1/T$.

From the analysis of the loop gain of the circuit in Figure 1 it is obtained that, by considering the closing delay of the switches 2 and 7 or 4 and 6, the voltage V_G at the inverting node of the amplifier 8 is $V_G = I * T * e^{sT} / C_r$, with the exponential factor being due to the above mentioned delay. Since $V_{cur} = V_G / (s * C_{int})$ and $I = K_c * V_{cur}$, a loop gain for small signals is obtained by:

$$G = \frac{T * e^{sT} * g_m * K_c}{s * C_r * C_{int}}$$

10

If the effect of the delay is not considered, the loop gain G is a transfer function having a single pole in the origin and a phase margin of 90° . The delay e^{sT} imposes that the frequency of unitary gain (this is the bandwidth of the circuit) is minor of a fraction of the frequency f :

15

$$BW = \frac{g_m * K_c}{2\pi f * C_r * C_{int}} \leq 0.25 * f$$

From this, there is obtained the relation:

$$f \geq \sqrt{\frac{2g_m K_c}{\pi C_{int} C_r}}$$

20

Therefore, by means of a frequency f that respects this inequality, a frequency/signal converter is obtained which is stable without compensating.

Alternatively it is possible to insert any integrator instead of the illustrated circuit portion that includes the transconductance amplifier 8 and the capacitor C_{int} .

25

Figure 4 shows a switching regulator that employs the converter of Figure 1. The regulator includes a MOS transistor HS having its drain terminal connected with an input voltage V_{in} ; its source terminal connected with a drain terminal of another

MOS transistor LS, with the cathode of a diode D1 whose anode is connected to ground, and with a terminal of an inductance L; and its gate terminal connected with a control device 100. The MOS transistor LS further has its gate terminal connected with the control device 100 and its source terminal connected with ground. The series
5 of a capacitor Cc and a resistor R is placed in parallel with a load LOAD and is connected between the other terminal of the inductance L and ground. A transconductance error operational amplifier 200 receives the output voltage Vout at the terminals of the load LOAD and a reference voltage Vref1. The transconductance error operational amplifier 200 provides a current I2 that is input to a current
10 comparator 300 that also receives a signal I1 representative of the current flowing through the inductance L that is obtained by a sensing resistor Rs (this is a resistor adapted to measure the current in the inductance L) and a slope current signal Islope provided by a device 101. The output signal S of the comparator 300 is input to the control device 100.

15 The device 101 receives a clock signal Cl and is adapted to determine the duty-cycle D (that is, the on time Ton and the off time Toff in a period Tsw fixed by the clock signal Cl), so as to drive the transistors HS and LS. The duty-cycle is varied in relation to the output signal S of the comparator 300.

The device 101 includes the frequency/signal converter of Figure 1 (described
20 above) from which a current signal proportional to the frequency f of the clock signal Cl is obtained. It flows through a circuit including a capacitor Cslope and a switch St arranged in parallel to the capacitor Cslope and driven so as to generate the slope current signal Islope.

In order to achieve a good stability for the switching regulator, the inclination
25 of the slope current signal Islope must be equal to about half the negative inclination of the signal I1 during the off time Toff (that is, the inclination of the discharge of the inductance L during the Toff time). This can be deduced by analyzing the stability of the regulator. In this case a perturbation Y is introduced in the current flowing through the inductance L in a certain clock period. At the successive clock period if
30 the regulator is stable the perturbation Y' in the current must be lower than Y. Figure

5 shows the theoretical signals I_{prog} and I_1 for calculating the inclinations, with I_{prog} being obtained by I_2 -Slope, the values of the perturbations Y and Y' , the value X obtained by the distance between the peaks of the currents I_1 obtained in the two successive clock periods, the rising inclination S_r and the falling inclination S_f of the current I_1 and the inclination Slope of the signal I_{prog} . It is obtained that $S_r + \text{Slope} = Y/X$, $S_f + \text{Slope} = Y'/X$ and $Y'/Y = (S_f - \text{Slope})/(S_r - \text{Slope})$. Also because $Y' < Y$ it must result $(S_f - \text{Slope})/(S_r - \text{Slope}) < 1$ from which $\text{Slope} > (S_f - S_r)/2$. Since $V_{out} = D \cdot V_{in}$ and because $S_r = (V_{in} - V_{out})/L$ this is $S_r = V_{in} \cdot (1 - D)/L$ and $S_f = V_{out}/L$ from which $S_f = V_{in} \cdot D/L$, it is obtained that $\text{Slope} > V_{in} \cdot (2D - 1)/(2 \cdot L)$. The most restrictive condition is obtained by imposing $D=1$ from which $\text{Slope} > V_{out}/(2 \cdot L)$ and also $\text{Slope} > S_f/2$.

Therefore it is achieved:

$$\text{Slope} = \frac{V_{out} R_s}{2L}$$

where the inclination of the slope current signal I_{slope} has been indicated with Slope.

15 The value of the inductance L is forever connected with the regulator switching frequency f_{sw} ; a higher switching frequency allows use of an inductance having a lower value, therefore $L = L_k / f_{sw}$ where L_k is a proportionality constant. From the above relation it is obtained that $\text{Slope} = K \cdot f_{sw}$ by indicating that $K = V_{out} \cdot R_s / (2 \cdot L_k)$. For this reason it is preferable to change the inclination of the slope compensation signal I_{slope} in a way proportional to the frequency, especially in the case of high switching frequencies, and the device 101 allows this to be achieved.

20 Figure 6 shows the waveforms of the signals I_1 and I_{prog} which were obtained through simulations of the circuit of Figure 4, with the inclination Slope of the slope current signal I_{slope} being imposed equal to at least half the highest discharge inclination S_f of the current flowing through the inductance L .

The present invention can be realized in hardware, software, or a combination of hardware and software. Any processor, controller, or other apparatus adapted for carrying out the functionality described herein is suitable. A typical combination of hardware and software could include a general purpose processor (or controller) with

EXPRESS MAIL NO. EV343427593US

a computer program that, when loaded and executed, carries out some or all of the functionality described herein.

While there has been illustrated and described what are presently considered to be the preferred embodiments of the present invention, it will be understood by those
5 skilled in the art that various other modifications may be made, and equivalents may be substituted, without departing from the true scope of the present invention. Additionally, many modifications may be made to adapt a particular situation to the teachings of the present invention without departing from the central inventive concept described herein. Furthermore, an embodiment of the present invention may
10 not include all of the features described above. Therefore, it is intended that the present invention not be limited to the particular embodiments disclosed, but that the invention include all embodiments falling within the scope of the appended claims.